AF/1280

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/651,385
Filing Date	August 29, 2000
First Named Inventor	Sanjay Dabral
Group Art Unit	2815
Examiner Name	Jose R. Diaz
Total Number of Pages in This Submission	38
Attorney Docket Number	42390P5258D

ENCLOSURES ***(check all that apply)***

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [X] Other Enclosure(s) *(please identify below):*

Check in the amount of $320
Return receipt postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Raul D. Martinez, Reg. No. 46,904 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Raul D Martinez
Date	August 11, 2003

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Lillian E. Rodriguez		
Signature	Lillian E. Rodriguez	Date	August 11, 2003

Based on PTO/SB/21 (03-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 08/11/2003.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 320.00

Complete if Known	
Application Number	09/651,385
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☐ Deposit Account

Deposit Account Number: 02-2666

Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

The Commissioner is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☒ Credit any overpayments

☒ Charge any additional fee(s) required under 37 CFR/1.16, 1.17, 1.18 and 1.20.

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims		- 20** =		X =	
Independent Claims		- 3 =		X =	
Multiple Dependent				=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple Dependent claim, if not paid
1204	84	2204	42	**Reissue independent claims over original patent
1205	18	2205	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

***or number previously paid, if greater, For Reissues, see below*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920 *	1804	920 *	Requesting publication of SIR prior to Examiner action	
1805	1,840 *	1805	1,840 *	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1404	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320.00
1403	280	2403	140	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	1809	375	Filing a submission after final rejection (37 CFR/1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR/1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
Other fee (specify)					

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 320.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Raul D. Martinez	Registration No. (Attorney/Agent)	46,904	Telephone	(310) 207-3800
Signature	Raul D Martinez			Date	08/11/03

Based on PTO/SB/17 (08-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlf) 08/11/2003.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

#15/ Appeal Brief 8/26/3 Smith

Our Ref. No.: 42390P5258D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	
Sanjay Dabral and Krishna Seshan	Examiner: Jose R. Diaz
Application No.: 09/651,385	
Filed: August 29, 2000	Art Unit: 2815
For: DIODE AND TRANSISTOR DESIGN FOR HIGH SPEED I/O	

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a check in the amount of $320.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(c). Please charge any additional amount due or credit any overpayment to Deposit Account No. 02-2666.

08/18/2003 HVUONG1 00000043 09651385
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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Sanjay Dabral and Krishna Seshan, the parties named in the caption, transferred their rights to that which is disclosed in the subject application through an assignment recorded on June 30, 1998 (9286/0474) to Intel Corporation of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation of Santa Clara, California is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will affect or be affected by the outcome of this appeal.

III. STATUS OF CLAIMS

Claims 20-29 are pending and stand rejected. Claims 20-29 are presented for appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed on March 10, 2003.

V. SUMMARY

Various methods are disclosed for forming an integrated circuit having a performance circuit in a first area of an integrated circuit substrate and a protection circuit coupled to the performance circuit and occupying a second area of the integrated circuit substrate (Appellants' specification, page 10, lines 2-7). Forming a performance circuit may include forming a transistor device with a drain region that is surrounded by a gate region (page 19, line 22-page 20, line 4). In various embodiments, the protection circuit (e.g., electrostatic ("ESD") diode) is separate from

the performance circuit (e.g., p-type metal oxide semiconductor ("PMOS") device). This separation ensures the best utilization of integrated circuit space (page 11, lines 8-18).

For example, among other advantages, the separation allows the performance circuit to be scaled up or down while maintaining the protection circuit at an ESD critical size. The reduction in excess area of either the protection circuit or the performance circuit reduces the capacitance while retaining the current handling capability of the protection circuit. A reduction of capacitance advantageously leads to faster transition times, which improves bus speeds (page 11, lines 18-25).

VI. ISSUES

The only issue involved in this appeal is as follows:

Whether Claims 20-29 are unpatentable under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,477,413 to Watt ("Watt").

VII. GROUPING OF CLAIMS

Appellants submit that the claims do not stand or fall together. Accordingly, Appellants group the claims as follows:

Group I	Claims 20 and 24-26
Group II	Claim 21-23
Group III	Claim 27-29

The reason for the independent patentability of the separate groups is discussed in detail below.

VIII. ARGUMENT

The Patent Office rejects Claims 20-29 under 35 U.S.C. § 102(b) as being anticipated by Watt.

A. Group I: Rejection of Claims 20 and 24-26 as Being Anticipated by Watt

In order to anticipate a claim, the relied upon reference must disclose every limitation of the claim. Among other limitations, independent Claim 20 recites forming a performance circuit in a first well of a substrate, forming a protection circuit in a second well of a substrate separate from the first well, and coupling the protection circuit to the performance circuit (emphasis added). Appellants submit that Watt fails to disclose all of these limitations.

In making the rejection (Final Office Action mailed March 10, 2003, page 2), the Patent Office relies on Watt to show forming performance circuit 54, 55 (of Figure 5) occupying first well 53, forming a protection circuit 52 occupying second well 51, and coupling the performance circuit to the protection circuit. In response, Appellants strongly disagree with the Patent Office's characterization of Watt as disclosing a performance circuit in a first well of a substrate and a protection circuit in a second well of a substrate.

Only a cursory review of Watt is necessary to see that nMOSFETs 54 and 55 within p-well 53 form the positive ESD protection component of an ESD protection circuit, and diode 52 within p-well 51 forms the negative ESD protection component of the ESD protection circuit (Col. 7, lines 2-9). Appellants submit that forming a positive component of a protection circuit in one well of a substrate and forming the negative component of the protection circuit in a second well within the substrate is not the same as forming a performance circuit in one well of a substrate and forming a protection circuit in a second well of the substrate, as recited in Appellants' independent Claim 20.

Beyond not meeting the claim language of Claim 20, a device constructed according to the teachings of Watt cannot achieve the advantages of a device constructed according to the method of Claim 20. For example, as described above in the Summary, the separation of the performance circuit from the protection circuit allows the performance circuit to be scaled up or down while maintaining the protection circuit at an ESD critical size. The reduction in excess area of either the protection circuit or the performance circuit reduces the capacitance while retaining the current handling capability of the protection circuit. A reduction of capacitance advantageously leads to faster transition times, which improves bus speeds. At least these advantages are neither

obtainable nor contemplated by Watt, which is directed at using NMOS transistors in one well and a diode in another well in order to prevent the lock-on condition that normally occurs after one transistor of a multi-finger structure snaps back (Abstract and Col. 2, line 64-Col. 3, line 1).

In maintaining the rejection (Final Office Action mailed March 10, 2003, page 3), the Patent Office first notes that during patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification, citing MPEP Section 2111. In view of the cited portion of the MPEP, the Patent Office refers Appellants' attention to Claim 27 wherein the term "performance circuit" includes a transistor having drain, gate, and contact regions. Based on the language of Claim 27, the Patent Office concludes that Watt fulfills the requirement for a performance circuit by showing a transistor (54, 55) in Figures 5 and 6 that has the required drain, gate, and contact regions. Finally, the Patent Office notes that, broadly speaking, the transistor (54, 55) can also be considered as a "performance circuit" since the transistor of Watt meets the definition presented by Appellants.

Given the disclosure of Watt (e.g., merely forming two different components of the same protection circuit within two different wells of a substrate), the plain meaning of Appellants' claim language, and the examples of "performance circuit" and "protection circuit" in Appellants' specification, one of skill in the art could not reasonably interpret, even in the broadest sense, that the term "performance circuit" could be used in the same manner as the term "protection circuit."

Moreover, Appellants believe that it is improper for the Patent Office to utilize language from Claim 27 relating to one specific embodiment of forming a performance circuit as being necessarily read into Appellants' independent Claim 20 in an attempt to anticipate Appellants' claims. However, even if such language is imported into Claim 20, Watt still fails to anticipate Appellants' claims. For example, regardless of the components used to form the performance circuit, Watt fails to disclose any type of performance circuit formed in a well separate from a protection circuit formed in another well of the substrate. Therefore, Appellants submit that, given the broadest reasonable interpretation consistent with the specification, Watt fails to disclose every limitation of Appellants' independent Claim 20.

In the Advisory Action dated June 9, 2003, the Patent Office states that Appellants' specification defines the term "performance circuit" as an NMOS or PMOS device (page 5, lines 13 and 14) but that the definition does not exclude an ESD structure as a performance circuit. From this, the Patent Office concludes that Appellants are arguing the impermissible importation of limitations or definitions into the claim.

In response, Appellants first note that although the cited portion of Appellants' specification refers to two specific examples of a performance circuit, Appellants' specification does not set forth any notion that the meaning of the term "performance circuit" can only be used to refer to those two devices (e.g., NMOS and PMOS devices). Moreover, it seems unreasonable for the Patent Office to conclude that since an ESD structure is not explicitly excluded from falling under the term "performance circuit," that an ESD structure must necessarily be included in the definition of performance circuit.

The MPEP does not contain any requirement that a specification set forth every item that must be excluded when interpreting a particular term or else anything not on the exclusionary list could be an acceptable interpretation of the term. Clearly, such a requirement would fall outside of the typical standard of giving each term in the claim its broadest reasonable interpretation in light of the specification. The notion that an ESD structure must necessarily fall within the meaning of "performance circuit" since it is not explicitly excluded by the specification is particularly disturbing when one considers that Appellants' specification is replete with references to an ESD structure as a protection circuit (page 10, lines 18-20; page 11, lines 8-12) but does not include a single instance in which an ESD structure is referred to as a performance circuit. Thus, Appellants submit that the Patent Office is attempting to give an unreasonably broad interpretation to the term "performance circuit" in light of the clear, plain meaning of the claim language and examples set forth in the specification.

Accordingly, Appellants respectfully request that the rejection of the claims of Group I be overturned.

B. Group II: Rejection of Claims 21-23 as Being Anticipated by Watt

Claim 21 is dependent on patentable independent Claim 20, discussed above, and those arguments are hereby incorporated regarding Claim 21. However, Claim 21 also contains at least one additional limitation that is not anticipated by Watt, which renders Claim 21 independently patentable over Watt. Specifically, Watt fails to disclose a method wherein forming a performance circuit includes forming a CMOS configuration, as recited in Claim 21.

In making the rejection, the Patent Office cites Figure 5 and Col. 9, lines 25-34 of Watt to show that the "performance circuit" of Watt can include a CMOS configuration. In response, Appellants note that the cited portion of Watt merely states that the invention (e.g., to place a positive ESD structure in one well and a negative ESD structure in another well) may be implemented in a wide array of technologies, including CMOS processing. However, placing two components of a single protection circuit in different wells, without any disclosure that the wells of the protection circuit will be separate from the well containing the CMOS, is not the same as forming a CMOS configuration in one well and forming a protection circuit in a different well, as recited in Claim 21. To arrive at the conclusion that Watt discloses the methodology recited in Claim 21 would consist of impermissible hindsight given that Watt lacks any description of the location of the protection circuit relative to a CMOS performance circuit. Thus, Watt fails to disclose every limitation of Claim 21.

Accordingly, the rejection of the claims of Group II should be overturned.

C. Group III: Rejection of Claims 27-29 as Being Anticipated by Watt

Claim 27 is dependent on patentable independent Claim 20, discussed above, and those arguments are hereby incorporated regarding Claim 27. However, Claim 27 also contains at least one additional limitation that is not anticipated by Watt, which renders Claim 27 independently patentable over Watt. Specifically, Watt fails to disclose forming a gate region surrounding a drain region of a transistor, as recited in Claim 27.

In making the rejection, the Patent Office refers to Figures 5 and 6 of Watt to show transistors 54, 55 with source regions 57a, 57b coupled to common drain 57e by gates 57c, 57d, respectively (Col. 7, lines 14-20). In response, Appellants note that only a cursory review of Figure 6 is necessary to see that gates 57c, 57d, considered alone or in combination, do not surround drain region 57e, as recited in Claim 27. Consequently, the structure disclosed by Watt cannot achieve the increased width to capacitance ratio (Appellants' specification, page 19, line 27-page 20, line 9) obtained by constructing a device according to the methodology of Claim 27, including a gate region that surrounds the drain region of a transistor. Thus, Watt fails to disclose every limitation of Claim 27.

Accordingly, the rejection of the claims of Group III should be overturned.

IX. CONCLUSION AND RELIEF

Based on the foregoing, Appellants request that the Board overturn the rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 8/11/03

Raul D. Martinez
Reg. No. 46,904

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Los Angeles, California 90025
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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 11, 2003.

Lillian E. Rodriguez 8-11-03

August 11, 2003

X. APPENDIX

The claims involved in this Appeal are as follows:

1.-19. Canceled

20. (Previously Amended) A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first well of an integrated circuit substrate;

forming a protection circuit occupying a second well of an integrated circuit substrate separate from the first well; and

coupling the protection circuit to the performance circuit.

21. (Previously Amended) The method of claim 20, wherein forming a performance circuit includes forming a CMOS configuration.

22. (Previously Amended) The method of claim 21, wherein coupling the protection circuit to the performance circuit includes coupling the protection circuit to a p-channel device of the CMOS configuration.

23. (Previously Amended) The method of claim 21, wherein forming a protection circuit includes forming a diode and coupling the protection circuit to the performance circuit includes coupling the diode to a p-channel device of the CMOS configuration.

24. (Previously Amended) The method of claim 20, wherein forming a protection circuit includes forming a unit diode, the unit diode comprised of a block of a doped region of the integrated circuit substrate occupying an area of the substrate sufficient to support a contact to the doped region, a junction region of the integrated circuit substrate surrounding the doped region, and a contact to the doped region.

25. (Previously Amended) The method of claim 24, the doped region being a first doped region of a first dopant in the second well of the substrate, the second well being doped with

a first concentration of a second dopant and the junction region separating the first doped region from the second well, wherein forming a protection circuit includes forming a third doped region in the second well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.

26. (Previously Amended) The method of claim 25, wherein forming a protection circuit includes forming a plurality of unit diodes.

27. (Previously Amended) The method of claim 20, wherein forming a performance circuit includes:

forming a unit transistor device having a drain region comprised of a doped region of the integrated circuit substrate occupying an area sufficient to support a contact to the doped region;

forming a gate region of the integrated circuit substrate surrounding the doped region; and

forming a contact to the doped region.

28. (Previously Amended) The method of claim 27, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a concentration of a second dopant and wherein forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor.

29. (Previously Amended) The method of claim 28, wherein forming a performance circuit includes:

forming a plurality of unit transistors.